AMENDMENTS TO THE SPECIFICATION

Please replace the abstract with the following amended abstract:

--A method and an apparatus to process read data return ~~has been disclosed~~ have been presented. In one embodiment, the method includes packing a cache line of each of a number of read data returns into one or more packets, splitting each of the one or more packets into a plurality of flits, and interleaving the plurality of flits of each of the plurality of read data returns. Other embodiments are described and claimed.--

Please replace paragraph [0051] with the following amended paragraph:

--In one embodiment, each read return is sent in a single packet. The chunks for two read returns sent in two separate packets appear time multiplexed on the interconnect 740. For example, referring to Figure [[7]] 6A, chunks from memory channel 0 are statically assigned to time slot 0 (710) and chunks from memory channel 1 are statically assigned to time slot 1 (720). In one embodiment, a read chunk from a memory channel is dynamically assigned to the first time slot that is open when the chunk becomes available to be forwarded to the interconnect 740. In one embodiment, the assignment remains valid for the transmission of the entire cache line returned in response to the corresponding read. In one embodiment, the idle/busy state of time slots can be maintained in a few bits, which may be updated when new assignments are made and a read transmission completes. Furthermore, it should be appreciated that the flit size may not be equal to the chunk size. If the flit size is larger than the chunk size, the memory controller hub may wait for more data chunk(s) from the memory channels before forming a flit. Alternatively, if the flit size is smaller than the chunk size, more flits are sent for each data chunk.--